Vertically Aligned ZnO Nanowires as Potential Nanoelectronic Building Blocks

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1. Introduction

Several studies have been performed on the fabrication and possible usage of quasi-one-dimensional nanostructures. An example of these nanostructures is ZnO nanowires (ZnO NWs). Horizontal ZnO NWs can be easily fabricated using chemical-vapor deposition. In this project, however, we focus on arrays of vertically-aligned NWs in a highly ordered template of anodic alumina oxide (AAO) membranes. Pulsed electrodeposition (PED) is the method used to literally deposit Zn into the pores of the membrane. Atomic-force microscope (AFM) technique is used to characterize the electron transport characteristics of the Zn NWs. In order to obtain ZnO NWs, annealing is used to oxidize the Zn nanowires. These ZnO NWs are building blocks for nanoscale field-effect transistors for logic gates, high density data storage and other ultra-high density integrated circuits.

2. The fabrication method

Aluminum is first mechanically and electrochemically polished, followed by a two-step anodization process. Gold/Titanium is then evaporated on one side of the membrane to serve as a working electrode. After removing the top aluminum layer, AAO membranes are left on the substrate and ready for the pulsed electrodeposition. Figure 1 shows a picture of the device before the PED:

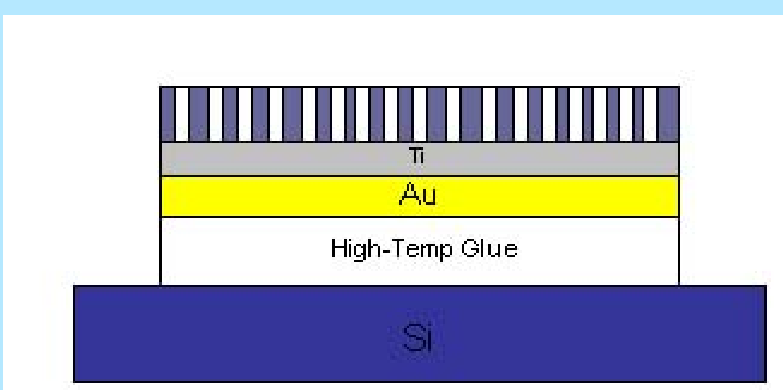

Fig.1:Schematic of the chip before PED

3. The pulsed-electrodeposition (PED)

PED is the method used to deposit Zn inside the holes of the AAO membranes. In aqueous deposition solutions, the high cathodic potentials cause some hydrogen evolution which can prevent the deposition. Hence, the delay time between pulses in the PED will compensate for the slow diffusion driven transport of Zn^{2+} into the pores, improving the filling factor of the holes, and consequently, the density of the NWs in the AAO membranes. Figure 2 shows SEM pictures of DC and pulsed electrodeposition methods and the improvement of the filling factor.

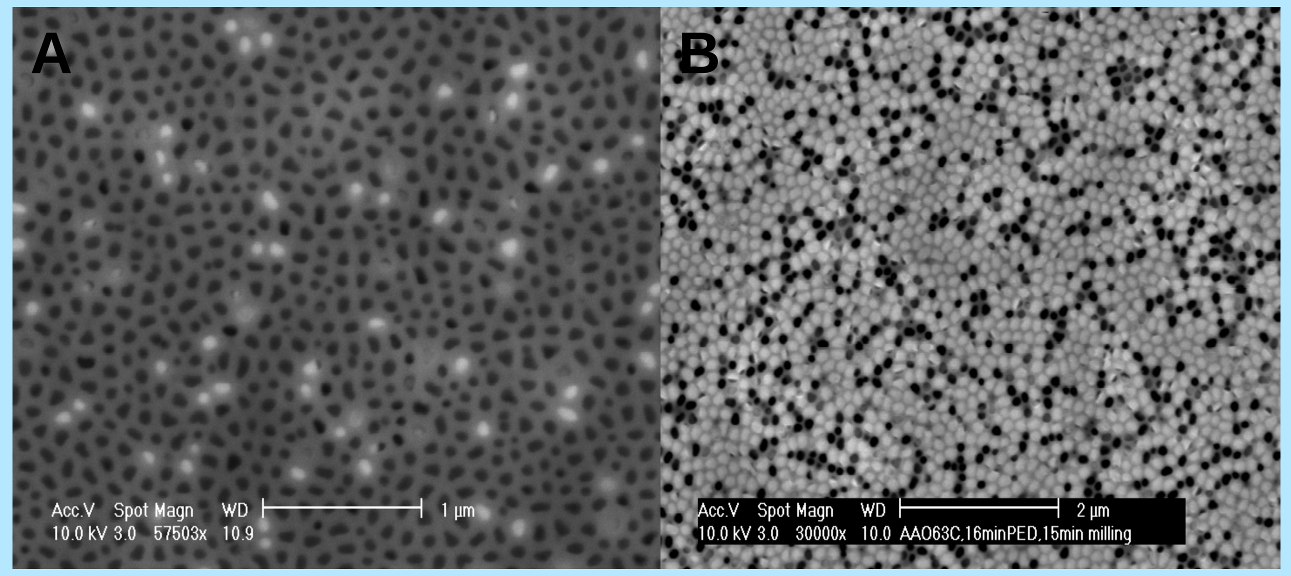

Fig.2: A. DC electrodeposition; B. PED. Notice how filling factor is much improved in B.

4. Characterization of Zn NWs

Atomic force microscope is used to characterize the morphology of the AAO membrane with Zn NWs inside (Figure 3) and the electron transport characteristic of individual Zn NW (Figure 4). The *I-V* curve in Figure 4.B shows indeed that there is a conducting channel between the tip of the probe and the bottom electrode. Furthermore, the curve shows that there is a Schottky contact between the tip and the Zn NWs because the top layer of Zn NW has been naturally oxidized. X-Ray Diffraction (XRD) spectra in Figure 5 also show Zn peaks, which is another proof of the existence of the Zn NWs.

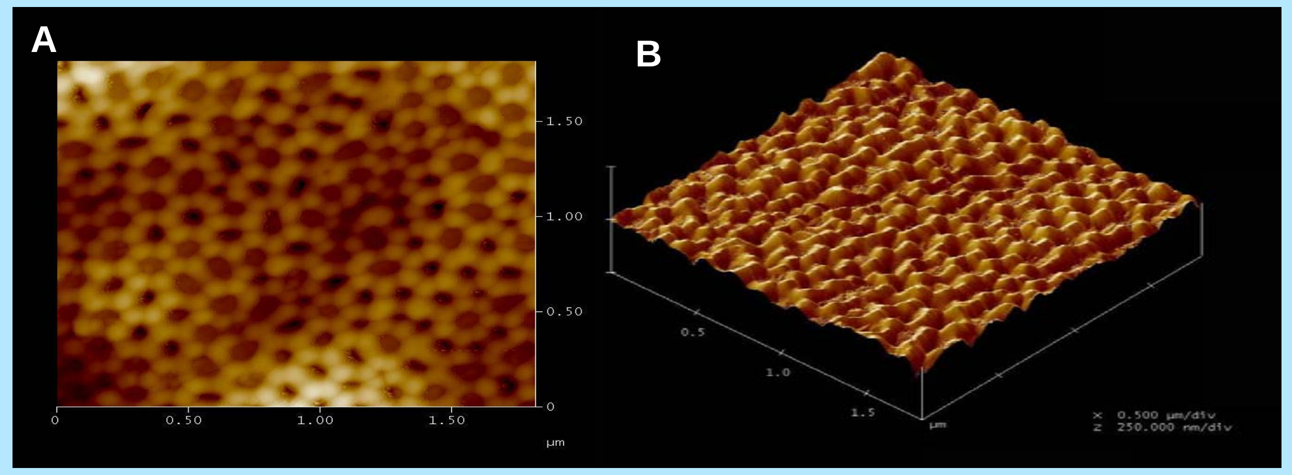

Fig.3: A. AFM picture of the AAO membrane filled with Zn nanowires. B. 3-D view of the same image. Density is approximately 70%-80%.

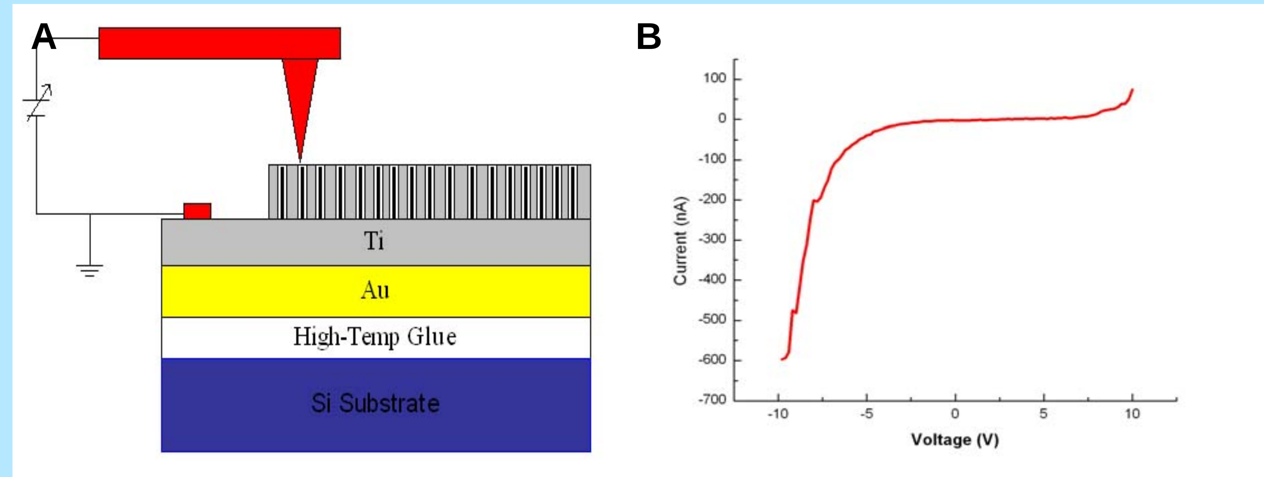

Fig.4: Schematic of the AFM measurement. The *I-V* curve in B shows a Schottky contact between the probe and the nanowire.

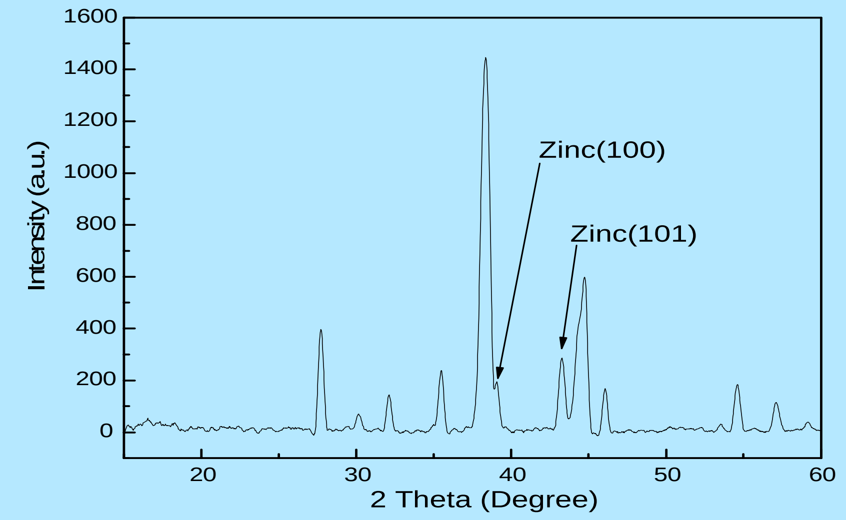

Fig. 5: XRD data confirming the presence of Zn in the chip.

5. Potential Building Blocks

The as grown Zn NWs are to be annealed and thus, oxidized to obtain a semiconductor behavior. Figure 6 from AFM shows the oxidization of Zn on the surface of the membrane after annealing for 2hrs. After obtaining ZnO NWs, top electrodes will be made using e-beam lithography, forming a standard three electrode device. With this structure, transistors are expected to be fabricated and used in integrated circuits and other nanoscale devices.

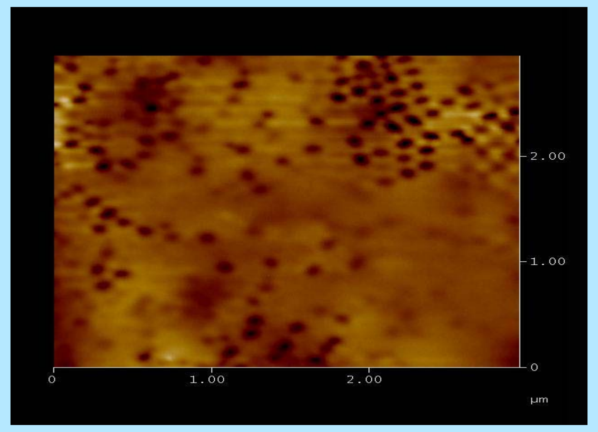

Fig. 6: Zn starting to become ZnO on the surface of the pores.

6.Conclusion

Zn NWs were fabricated in highly ordered AAO membranes. PED is used to deposit Zn in the holes of the membranes. ZnO NWs are expected to form after the annealing process, creating the desired semiconductor behavior. Top electrodes will be evaporated, and transistors will be made out of the vertically aligned ZnO NWs, which will serve as potential building blocks for nanoscale devices.

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